REMARKS

Reconsideration and allowance of the above-referenced application are respectfully requested.

Upon entry of this amendment, claims 1-7, and 15-26 will remain in the application.

Specification

The specification stands objected to for failing to include a "summary" section. This objection is respectfully traversed. The cited rule states what a specification should include, and falls short of making a summary section mandatory. Intel Corporation has taken the position that they prefer to omit summaries in their applications. Since compliance with Rules 73 and 77 is entirely voluntary, it is respectfully suggested that the application is totally complete without a summary section, and therefore the requirement for a summary section is respectfully traversed.

Claim Rejections - 35 USC § 112

Claim 1 was rejected for under 35 U.S.C. 112, second paragraph, as allegedly being indefinite.

Claim 1 has been amended to clarify that the register set has a random access memory (RAM) architecture. Each bank in the register has a dual-port RAM construction, such that each bank is capable of performing a read and write to two different words within its bank in the same clock cycle (see page 22, lines 30-31). Therefore, a register file with two banks would be able to perform four accesses (two per bank) each cycle.

Claim Rejections - 35 USC § 102

Claims 1-5 and 15-22 were rejected under 35 U.S.C. 102(b) as allegedly being anticipated by Parady (U.S. Patent No. 5,933,627).

Applicants teach a general purpose register set with a dual-ported RAM architecture and including a number of banks, each bank having two ports and being partitioned into windows to accommodate a number of threads. The RAM architecture may enable smaller cells, and hence more registers, than a typical register file architecture.

Parady discloses a typical register file architecture, e.g., integer registers 48 in FIG. 1. The integer registers 48 include 8 windows for 4 threads and include 10 ports. However, in the embodiment described the Specification, the register file set having the dual-ported RAM architecture supports four threads (page 3, line 18), 8 windows (Figure 6), and only requires 4 ports (two for each of banks A and B). Furthermore, a search of the text of Parady indicates that the terms "random access memory" and "RAM" are not even mentioned.

Parady does not disclose or suggest a register file set having a two-ported RAM architecture. Accordingly, Applicants submit that independent claims 1, 15, and 19, and their dependencies, are allowable.

Claim Rejections - 35 USC § 103

Claims 6-10 and 23-25 were rejected under 35 U.S.C. 103(a) as allegedly being unpatentable over Parady in further view of Waldspurger et al, "Register Relocation: Flexible Contexts for Multithreading".

Claims 6-10 and 23-25 depend from independent claims 1 and 19, respectively. Accordingly, Applicants submit that these

claims are allowable for the reasons given above and for their additional limitations.

Enclosed is our check in the amount of $420 for the Petition for Extension of Time fee. Please apply any other charges or credits to deposit account 06-1050.

Respectfully submitted,

Date: August 9, 2004

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